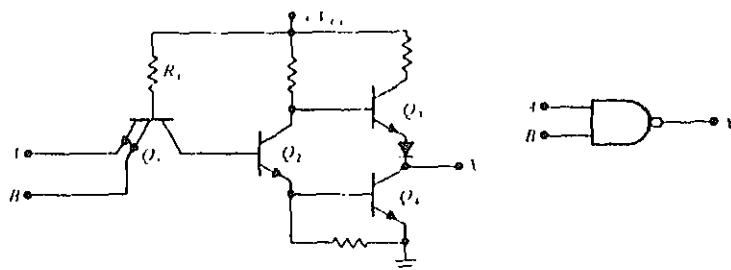


ASSIGNMENT BOOK

FOR

ADVANCED FIRST-TERM AVIONICS COL

CLASS A1
C-100-2010



TTL NAND

UNIT V

CNTT-M 1629 Rev. 12/84

PREPARED BY

NAVAL AIR TECHNICAL TRAINING CENTER
NAVAL AIR STATION MEMPHIS
MILLINGTON, TENNESSEE

PREPARED FOR

CHIEF OF NAVAL TECHNICAL TRAINING

JANUARY 1983

purpose of this Assignment Book is to assist you through
uter Theory and Troubleshooting, Unit 5, of the Advanced
Avionics Course. The proper use and completion of the
gnments contained in this book will greatly enhance your
rstanding of the material presented in this unit.

table of contents lists the page numbers for safety noti
s schedules, homework schedules, learning objectives, and
gnment Sheets that will further enhance your abilities as
electronics technicians.

SAFETY NOTICE

As a Navy electronics technician, you will be required to perform safe and efficient maintenance on various types of electronic equipment. Not only your life, but the lives of many others depend on your being safety conscious at all times. It is the responsibility of all Navy and Marine Corps personnel to prevent accidents. This can be done if everyone develops conscientious safety habits and observes all precautions when performing maintenance of any type.

Assignment Book has been prepared for you to use while you attend the Advanced First-Term Avionics Course. Remember that homework is mandatory. When you are in class, the information provided is information you will need in performing your Navy assignments. This volume contains the homework assignments that will direct your efforts.

Unit V is two weeks long, and starts in the middle of the first week of the eighth week. The periods run from 317 to 396, with the period finishing half-way through the last day of the tenth week.

The schedule is as follows:

TOPIC NO.	TYPE	PERIOD	TOPIC
EIGHTH WEEK			
Fifth Day			
4.17	Class	313	Unit/Module Test: Criteria
		314	Written Examination
		315	
		316	
5.1	Class	317	Introduction to Digital
		318	
5.2	Class	319	Mathematics of Digital
		320	
NINTH WEEK			
First Day			
5.2	Class	321	Mathematics of Digital
		322	
		323	
		324	
5.3	Class	325	Basic Logic Gate Interpre
		326	
		327	
		328	
Second Day			
5.3	Class	329	Basic Logic Gate Interpre
		330	
5.4	Class	331	Introduction to the COM-T
		332	Computer and Organization
		333	
5.5	Class	334	COM-TRAN Ten Logic and Da
		335	
		336	

Third Day

5.6	Class	337	COM-TRAN Ten Software
		338	
		339	
		340	
		341	
		342	
		343	
		344	

Fourth Day

5.7	Class	345	COM-TRAN Ten Hardware
			Diagram Data Flow
		346	
		347	
		348	
		349	
		350	
		351	
		352	

Fifth Day

5.7	Class	353	COM-TRAN Ten Hardware
			Diagram Data Flow
		354	
		355	
		356	
		357	
		358	
		359	
		360	

TENTH WEEK

First Day

5.7	Class	361	COM-TRAN Ten Hardware
			Diagram Data Flow
		362	
		363	
		364	
		365	
		366	
		367	
		368	

TOPIC NO.	TYPE	PERIOD	TOPIC
Second Day			
5.8	Lab	369 370 371 372	COM-TRAN Ten Data Flow An
5.9	Lab	373 374 375 376	COM-TRAN Ten Fault Isolat
Third Day			
5.9	Lab	377 378 379 380 381 382 383 384	COM-TRAN Ten Fault Isolat
Fourth Day			
5.9	Lab	385 386 387 388	COM-TRAN Ten Fault Isolat
	Lab	389 390 391 392	Unit/Module Test: Criter Performance Test
Fiftn Day			
5.9	Class	393	Unit/Module Test: Criter
5.10	Class	394 395 396	Written Test Within - Course Comprehen I, Written Examination and
6.1	Class	397 398 399 400	Introduction to Airborne P (Demo)

of the Assignment Sheets listed below shall be turned in.
Each Assignment Sheet will be checked by an instructor for completeness and correctness. Failure to turn in an Assignment Sheet could result in disciplinary action.

Assignment Sheet	Period Due
1.1A	321
2.1A	329
3.1A	337
4.1A	337
5.1A	337
6.1A	345
7.1A	369

TERMINAL OBJECTIVE

- 11.0 Isolate an instructor-induced malfunction (under limited supervision) in an avionics, general purpose digital computer training device to a weapons replaceable assembly, a stage, and a component and record results on job sheets. Test equipment will be provided. Performance must be accomplished in accordance with COM-TRAN Ten Technical Operations Manual M104. All general and personnel safety precautions must be observed, in accordance with OPNAVINST 5101.2 series.

ENABLING OBJECTIVES

- 11.1 EXTRACT troubleshooting and performance data from circuit block and logic diagrams of a general purpose digital computer training device. All circuit performance and operating characteristics will be documented on job sheets in accordance with specifications contained in COM-TRAN Ten Technical Operations Manual M104, Vol. I.
- 11.2 PERFORM visual inspections on an avionics general purpose digital computer training device for physical defects, security, integrity, and proper installation and REPAIR results on a job worksheet. Performance must be accomplished in accordance with procedures outlined in TRAN Ten Technical Operations Manual M104, Vol. I.
- 11.3 PERFORM operational and minimum performance checks (under limited supervision) on an avionics general purpose digital computer training device and RECORD results on job sheets. Necessary test equipment will be provided. Performance must be accomplished in accordance with Ten Technical Operations Manual M104, Vol. I. All safety precautions must be observed in accordance with OPNAVINST 5101.2 series.
- 11.4 ISOLATE an instructor-induced malfunction (under limited supervision) on an avionics general purpose digital computer training device to a weapons replaceable assembly, a stage, and a component and record results on job sheets. Test equipment will be provided. Performance must be accomplished in accordance with TRAN Ten Technical Operations Manual. All safety precautions must be observed in accordance with OPNAVINST 5101.2 series.

DOCUMENT, on the VIDS/MAF, all necessary corrective action required in a given maintenance situation to restore avionics general purpose digital computer training device to an operational condition. Documentation must include ordering and receipt of parts. All documentation must be legible and in accordance with OPNAVINST 4790.2 series 1.

FRONT MATTER

FOREWORD	
SAFETY NOTICE	
HOW TO USE THIS ASSIGNMENT BOOK	
UNIT V CLASS SCHEDULE	
UNIT V HOMEWORK SCHEDULE	
UNIT V LEARNING OBJECTIVES	

ASSIGNMENTS

ASSIGNMENT SHEET 5.1.1A	
ASSIGNMENT SHEET 5.2.1A	
ASSIGNMENT SHEET 5.3.1A	
ASSIGNMENT SHEET 5.4.1A	
ASSIGNMENT SHEET 5.5.1A	
ASSIGNMENT SHEET 5.6.1A	
ASSIGNMENT SHEET 5.7.1A	

INTRODUCTION TO DIGITAL COMPUTERS

INTRODUCTION

The purpose of this assignment is to familiarize you with principles of a digital computer system. Once this knowledge has been mastered, you will be able to troubleshoot a basic digital computer system.

LESSON TOPIC LEARNING OBJECTIVES

- 11.1 EXTRACT troubleshooting and performance data from block and logic diagrams of a general purpose digital computer training device. All circuit performance and operating characteristics will be documented on drawings in accordance with specifications contained in Control Technical Operations Manual M104, Vol. I.
- 11.1.1. SELECT, from a given list, the definition of the major classes of computers.
- 11.1.2. SELECT, from a given list, the computer unit that determines the overall speed of a digital computer.
- 11.1.3. SELECT, from a given list, the computer unit that performs an explicit or implicit operation.
- 11.1.4. SELECT, from a given list, the computer instructions that are used in the control unit.
- 11.1.5. SELECT, from a given list, the definition of "random access."
- 11.1.6. SELECT, from a given list, the definition of a "Volatile memory device."
- 11.1.7. SELECT, from a given list, the computer units that are included in the central processing unit of a digital computer.
- 11.3 PERFORM operational and minimum performance check (under limited supervision) on an avionics general purpose computer training device and RECORD results on drawing sheets. Necessary test equipment will be provided. Performance must be accomplished in accordance with Control Technical Operations Manual M104, Vol. I. All safety precautions must be observed in accordance with OPNAVINST 5050.1 (series).

supervision/ on an avionics general purpose digital training device to a weapons replaceable assembly shop replaceable assembly, a stage, and a component RECORD results on job sheets. Test equipment will be provided. Performance must be accomplished in accordance with the COM-TRAN Ten Technical Operations Manual. All safety precautions must be observed in accordance with 5101.2 (series).

STUDY ASSIGNMENT

Study Information Sheet 5.1.1I and Notetaking Sheet 5.1.1A.
Complete Assignment Sheet 5.1.1A.

STUDY QUESTIONS

1. The two classes of computers are
 - a. _____
 - b. _____
2. What are the two types of digital computers?
 - a. _____
 - b. _____
3. What are the four capabilities of a digital computer?
 - a. _____
 - b. _____
 - c. _____
 - d. _____
4. Name the five basic units of a general-purpose digital computer?
 - a. _____
 - b. _____
 - c. _____
 - d. _____
 - e. _____

- a. _____
- b. _____
- c. _____

6. Which units determine the overall speed of a computer?

- a. _____
- b. _____

7. List the three basic functions of the control

- a. _____
- b. _____
- c. _____

8. Name the four instructions used in the control

- a. _____
- b. _____
- c. _____
- d. _____

9. What are the two categories of arithmetic operations?

- a. _____
- b. _____

10. Define the terms "volatile" and "nonvolatile" in relation to a memory device.

- a. _____
- b. _____

- a. _____
- b. _____
- c. _____
- d. _____
- e. _____

12. What are the two modes of access used in a memory?

- a. _____
- b. _____

13. The terms "on line" and "off line" refer to which units?

- a. _____
- b. _____

MATHEMATICS OF DIGITAL COMPUTERS

INTRODUCTION

The purpose of this assignment is to provide you with understanding of binary arithmetic, conversion, numberification, complement arithmetic, computer arithmetic terminology used to describe machine and mathematical. With this knowledge, the student will be able to troubleshoot a basic digital computer system.

LESSON TOPIC LEARNING OBJECTIVES

- 11.3.1. SELECT, from a given list, the definition of binary arithmetic.
- 11.3.2. SELECT, from a given list, the common number used in digital computers.
- 11.3.3. CONVERT specified decimal numbers to their octal, and hexadecimal equivalents.
- 11.3.4. CONVERT specified octal and hexadecimal numbers to their decimal and binary equivalents.
- 11.3.5. PERFORM, with given binary numbers, the indicated arithmetic operations.
- 11.3.6. SELECT, from a given list, the primary advantage of complement arithmetic.
- 11.3.7. PERFORM, with given binary numbers, the 2's complement method of subtraction and addition.
- 11.3.8. SELECT, from a given list, the method used to represent negative numbers in the COM-TRAN Ten.
- 11.3.9. SELECT, from a given list, the method of multiplication used in the COM-TRAN Ten.
- 11.3.10. SELECT, from a given list, the method of division used in the COM-TRAN Ten.

STUDY QUESTIONS

1. Match the following terms with their definitions, B.

A

- | | |
|----------------------|---------------------|
| a. _____ Radix | f. _____ Modulus |
| b. _____ Radix point | g. _____ Complement |
| c. _____ Bit | h. _____ Open-end |
| d. _____ Byte | i. _____ Closed-end |
| e. _____ Word | j. _____ Positional |

B

1. A number system in which the value of a digit upon the position of the digit within a number
2. The number of discrete conditions a device or indicate.
3. A set of bits that occupies one storage location.
4. The number of characters used in a number system.
5. The process by which a carry or borrow generated from the most-significant digit is brought to the least significant digit and is added.
6. A binary digit, either a 0 or 1.
7. The dividing point between whole numbers and fractions.

carry or borrow generated from the most-significant digit is brought to the least significant digit and is added.

the modulus or higher power of the radix to represent the negative value.

bits acted upon as a unit, such as a byte or word.

- a. A _____
- b. B _____
- c. C _____
- d. D _____
- e. E _____
- f. F _____

3. Convert the following decimal numbers to binary, octal, and hexadecimal.

	Binary	Octal	Hexadecimal
a. 69_{10}	_____	_____	_____
b. 36_{10}	_____	_____	_____
c. 77_{10}	_____	_____	_____
d. 127_{10}	_____	_____	_____
e. 46_{10}	_____	_____	_____

4. Convert the following binary numbers to decimal.

- a. 11011001_2 _____
- b. 111111_2 _____
- c. 101011_2 _____
- d. 1110101_2 _____

5. Convert the following octal numbers to decimal.

- a. 327_8 _____
- b. 734_8 _____
- c. 26_8 _____

- d. $7D_{16}$ _____
- e. $14C_{16}$ _____
- f. $7E_{16}$ _____
- g. $5A_{16}$ _____
- h. $1BA_{16}$ _____
- i. $3DE_{16}$ _____

7. Convert the following octal numbers to binary.

- a. 307_8 _____
- b. 47_8 _____
- c. 147_8 _____

8. Convert the following hexadecimal numbers to binary.

- a. 59_{16} _____
- b. 36_{16} _____
- c. $A6_{16}$ _____
- d. $F7_{16}$ _____
- e. $24C_{16}$ _____
- f. $C9_{16}$ _____
- g. $AB3_{16}$ _____

9. Convert the following binary numbers to hexadecimal

- | | |
|-------------------------|-------------------------|
| a. 11011001_2 _____ | e. 00101101_2 _____ |
| b. 10100111_2 _____ | f. 110101101_2 _____ |
| c. 11110101_2 _____ | g. 1110111011_2 _____ |
| d. 1011011011_2 _____ | h. 110110110_2 _____ |

a. 101.10011
 $+11101001$

c. 00111
 +10101

b.
$$\begin{array}{r} 10010 \\ +01010 \\ \hline \end{array}$$

d.
$$\begin{array}{r} 01011101 \\ +11101110 \\ \hline \end{array}$$

11. Subtract the following binary numbers.

a. $\begin{array}{r} 1101 \\ -0110 \end{array}$

c. $\begin{array}{r} 11111011 \\ -10111110 \\ \hline \end{array}$

b. $\begin{array}{r} 101101 \\ -011010 \\ \hline \end{array}$

d. $\begin{array}{r} 11101001 \\ -01110110 \\ \hline \end{array}$

12. Multiply the following binary numbers.

a.
$$\begin{array}{r} 101101 \\ \times 111 \\ \hline \end{array}$$

$$\begin{array}{r} c. \quad 11001101 \\ \quad \times 10011 \\ \hline \end{array}$$

b.
$$\begin{array}{r} 11011011 \\ \times 10110 \\ \hline \end{array}$$

$$\begin{array}{r} \text{d.} \quad 11011 \\ \times 101 \\ \hline \end{array}$$

13. Divide the following binary numbers.

a. $11110 \div 101 =$ _____

c. $11101110 \div 1101$

b. $0111 \div 010 =$ _____

d. $0110101 \div 011$

14. What are the two methods of complement arithmetic?

a. _____

b. _____

- a. 0110101_2 _____
- b. 011101110_2 _____
- c. 101011_2 _____

16. Write the following binary numbers in 2's complement

- a. 01011101_2 _____
- b. 01101110_2 _____
- c. 01111111_2 _____
- d. 00010010_2 _____

17. What method of complementation is used in the Com-Tr to represent negative numbers?

18. Write the negative hexadecimal value of the following complemented binary numbers.

- a. $1000\ 0001_2$ _____
- b. $1110\ 1111_2$ _____
- c. $1111\ 1111_2$ _____
- d. $1101\ 0001_2$ _____
- e. $1000\ 0000_2$ _____

19. Convert the following decimal numbers to binary and using the 1's complement.

- a. -14 -----
 -6 -----

- c. -69 -----
 $+49$ -----

- b. $+23$ -----
 -19 -----

tract, using the 1's complement.

a. -23 -----
 +19 -----

b. +16 -----
 + 5 -----

c. +54 -----
 -36 -----

. Convert the following decimal numbers to binary and add using the 2's complement.

a. -19 -----
 +20 -----

b. -17 -----
 -10 -----

c. +19 -----
 -11 -----

. Convert the following decimal numbers to binary and subtract, using the 2's complement.

a. +15 -----
 +10 -----

b. +19 -----
 -11 -----

c. -19 -----
 + 9 -----

- b. Repetitive addition
 - c. Addition and shift right
 - d. Shift left
24. The COM-TRAN Ten uses what method of division?
- a. Repetitive subtraction
 - b. Subtract and shift right
 - c. Shift left
 - d. Shift left and subtract
25. Convert the following binary numbers to Gray code
- a. 0010_2 _____
 - b. 0110_2 _____
26. Convert the following Gray code numbers to binary
- a. 0111 _____
 - b. 0011 _____

BASIC LOGIC GATE INTERPRETATION

INTRODUCTION

The purpose of this assignment is to provide you with a basic knowledge of the various types of logic gates that are used to make up a digital computer system. A basic understanding of logic function, operation, and application of the various logic gates will provide you with the knowledge that will be required to troubleshoot the COM-TRAN Ten digital computer system successfully.

LEARNING TOPIC LEARNING OBJECTIVES

- .9. SELECT, from a given list, the definition of a logic symbol.
- .10. SELECT, from a given list, the statement describing positive logic.
- .11. SELECT, from a given list, the purpose of the negative indicator system.
- .12. SELECT, from a given list, the truth table that describes the logic function of a specified logic gate.
- .13. MATCH, from given lists, the logic gate equivalent to the logic gate that produces the same truth table.
- .14. SELECT, from a given list, the statement describing operation of an RS latch.
- .15. SELECT, from a given list, the statement describing operation of a "D" edge-triggered flip-flop.
- .16. SELECT, from a given list, the statement describing operation of a single-shot multivibrator.
- .17. SELECT, from a given list, the function of a wire-OR gate.

HOMEWORK ASSIGNMENT

Review Notetaking Sheet 5.3.1N and complete Assignment Sheet 5.3.1A.

1. What is the definition of a logic symbol?

2. What is the difference between a basic logic diagram and a detailed logic diagram?

3. Define the term "positive logic."

4. When using the negation indicator system, the bubble on the input of a logic symbol indicates what?

a. Input is statically _____.

b. Active input is _____.

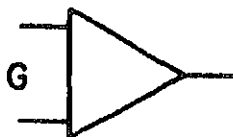
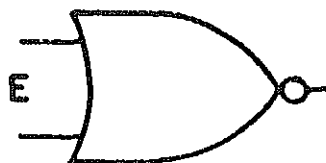
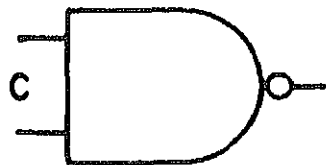
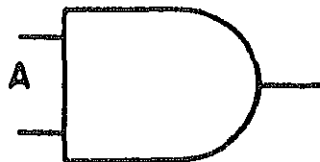
5. When using the negation indicator system, the bubble on the output of a logic symbol indicates what?

a. Output is statically _____.

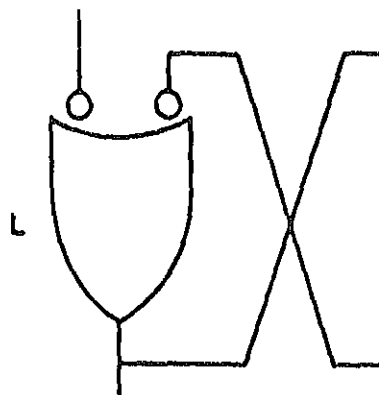
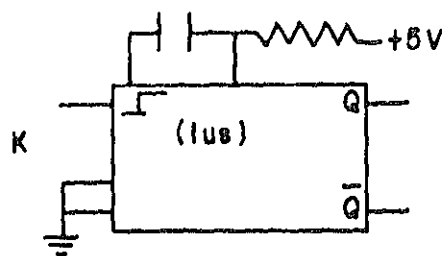
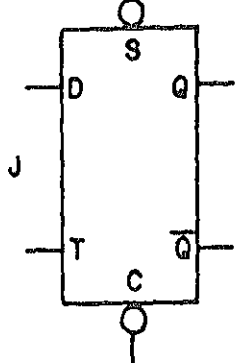
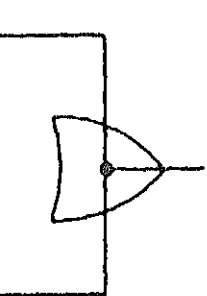
b. Active output is _____.

6. Match each term listed in Column A with the symbol in Column B that it describes.

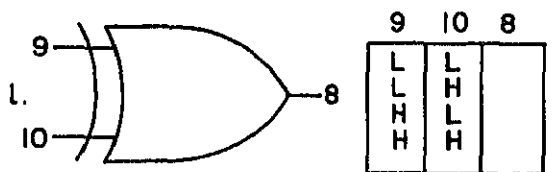
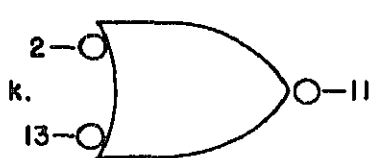
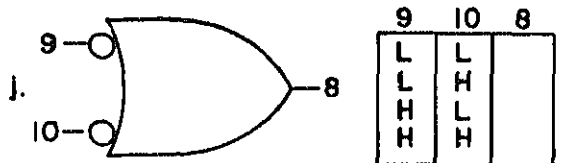
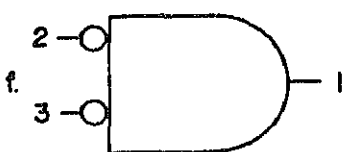
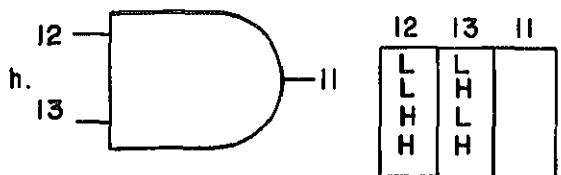
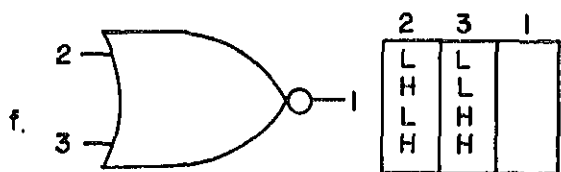
- | <u>Column A</u> | <u>Column B</u> |
|------------------------------|-----------------|
| a. _____ NOR gate | |
| b. _____ Inverter | |
| c. _____ Amplifier | |
| d. _____ AND gate | |
| e. _____ Exclusive OR | |
| f. _____ NAND gate | |
| g. _____ Wired OR | |
| h. _____ Positive AND driver | |
| i. _____ R-S latch | |
| j. _____ Type "D" Flip-Flop | |
| k. _____ Single-shot | |
| l. _____ OR gate | |



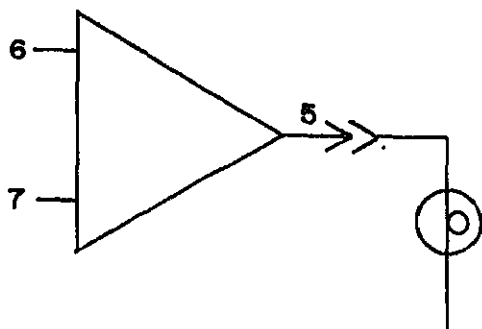
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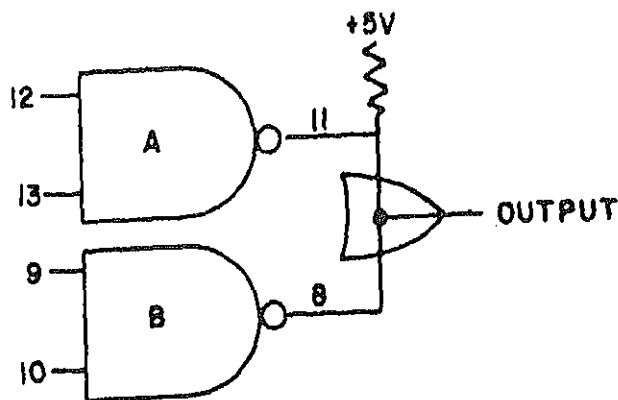
7. Complete the truth tables for the following Logic gates.



8. What is the condition of the lamp below with a +5 V a applied to the positive AND driver?

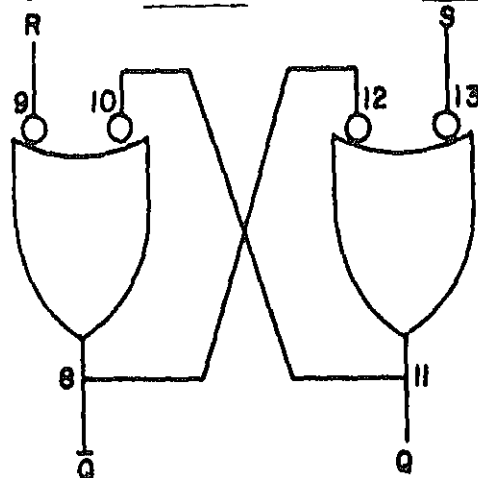


. With two HIGHS applied to NAND gate A what is the output of the wired OR?



D. With a LOW applied to pin 9 and a HIGH applied to pin 13, what is the logic level at the following pins of the R-S latch?

a. Pin 8 _____ Pin 12 _____ Pin 10 _____ Pin 11 _____

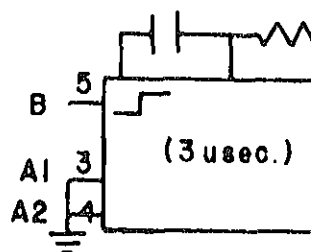
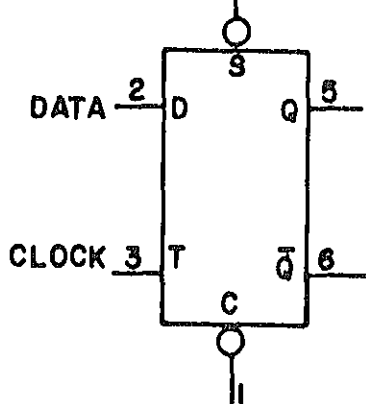


Refer to the "D" edge-triggered flip-flop to answer questions 11, 12, and 13.

1. What single input will cause the flip-flop to change state when the Q-output is HIGH?

2. What will the Q-output be when the "D" input is LOW and a pulse is applied?

input level for the SET and CLEAR inputs



Type "D" edge-triggered flip-flop

Sim

Refer to the single-shot to answer questions 14, 17.

14. What input trigger is required to produce a positive-going edge on the Q-output?

15. When the single-shot is triggered, how long will it stay in the unstable state?

16. What determines the pulse width of the Q-output?

17. The single-shot will be triggered on what portion of the input trigger?

INTRODUCTION

The purpose of this assignment sheet is to provide you with basic knowledge of the COM-TRAN Ten computer. A basic understanding of the function and purpose of the control registers of the COM-TRAN Ten will provide you with the knowledge that will be required to troubleshoot the COM-TRAN Ten computer.

LESSON TOPIC OBJECTIVES

- 11.2.11 SELECT, from a given list, the characteristics of the COM-TRAN Ten memory unit.
- 11.3.12 SELECT, from a given list, the arithmetic operations performed by the arithmetic logic unit.
- 11.3.13 MATCH the control panel switches with the statements that describe their functions.
- 11.3.14 MATCH the modes of operation with the statements that describe their functions.
- 11.3.15 MATCH the counters and registers with the statements that describe their functions.
- 11.3.16 SELECT, from a given list, the function of the status indicators.
- 11.3.17 EXPLAIN the function of the condition code indicators by selecting the correct description from a list of statements.
- 11.3.18 SELECT, from a given list, the statement that describes the purpose of the wait light.
- 11.3.19 SELECT, from a given list, the statement that describes the purpose of the status indicators.
- 11.3.20 SELECT, from a given list, the statement that describes the acquisition phase of an instruction.
- 11.3.21 SELECT, from a given list, the statement that describes the execution phase of an instruction.

STUDY QUESTIONS

Answer the following questions:

1. What is the capacity of each memory level?
 - a. 1024 8-bit words:
 - b. 255 8-bit words:
 - c. 256 8-bit words:
 - d. 1023 8-bit words:

2. List the four arithmetic operations performed by the arithmetic logic unit.
 - a. _____
 - b. _____
 - c. _____
 - d. _____

3. The input section of the control panel consists of _____ switches?
 - a. _____
 - b. _____
 - c. _____

describes its function or purpose.

- | | |
|------------------------------------|--|
| ___ (1) Power switch | a. Set up computer to read data into memory from the teletype. |
| ___ (2) Lamp test | b. Computer will attempt to execute an invalid instruction. |
| ___ (3) Manual data entry switches | c. Sets up computer to write from memory to teletype. |
| ___ (4) Reset switch | d. Used to read data into or out of memory in alphabetical letters, characters, or decimal digits. |
| ___ (5) HEX data switches | e. Computer will continue to operate when the Q-register exceeds a +127 or a -128. |
| ___ (6) Register select switches | f. Applied power to the computer. |
| ___ (7) RD switch | g. Computer will continue to operate when the A-register exceeds a +127 or a -128. |
| ___ (8) WT switch | h. Stops the computer clock. |
| ___ (9) REXMT off switch | i. Used to enter data into I-register in binary form. |
| ___ (10) HEX mode switch | j. Computer will acquire and execute instructions by internal controls. |
| ___ (11) ALPHA mode switch | k. Clears all registers. |
| ___ (12) Clear switch | l. Computer will stop after executing one instruction acquiring the next instruction. |
| ___ (13) Stop switch | m. Checks all lamps on display panel and the I-register select switches. |
| ___ (14) Start switch | n. Computer will stop after acquisition phase of an instruction. |
| ___ (15) PROG mode switch | o. Automatically sets up computer to execute a manual output instruction. |
| ___ (16) INST mode switch | |
| ___ (17) A/E mode switch | |
| ___ (18) DIST mode switch | |
| ___ (19) RPT mode switch | |
| ___ (20) Sense mode switch | |
| ___ (21) INST error bypass | |
| ___ (22) ADD error bypass | |
| ___ (23) DIV error bypass | |
| ___ (24) Read INTRPT switch | |

- q. Starts computer clock.
- r. Resets the I-register.
- s. Used to repeat any mode
tion except program mode
- t. Automatically sets up co
execute a manual input i
tion.
- u. Used to enter data in he
decimal form.
- v. Computer will stop after
or DPA pulse.
- w. Turns teletype printer o
- x. Causes computer to perfo
in the program when a sk
struction is received.
- y. Used to read into or out
memory in hexadecimal fo

5. Match each of the following counters/registers with the
ments that describes its purpose.

- | | |
|----------------------|---|
| ___ (1) A-register | a. Holds the count of the
process steps to be per
a multiply instruction. |
| ___ (2) B-register | |
| ___ (3) C-register | b. Holds the multiplier pr
execution of a multiply
tion. |
| ___ (4) D-register | |
| ___ (5) S-register | c. Controls the sequence o
timing pulse. |
| ___ (6) M-register | |
| ___ (7) P-register | d. Holds the address of th
instruction to be acqui
memory. |
| ___ (8) Q-register | |
| ___ (9) X-register | e. Holds the sum after the
of an ADD instruction. |
| ___ (10) I-register | f. Holds the product after
execution of a multiply
instruction. |
| ___ (11) AQ register | |

- h. Holds the address of the operation being executed.
 - i. Holds the subtrahend during execution of a subtraction.
 - j. Used for indexing the operand address.
 - k. Used to hold the data to be input manually into any register.
6. The condition codes reflect the status of what register after completion of all but the MPY, DIV, SRA, and SLA instructions?
- a. AQ-register
 - b. B register
 - c. A register
 - d. Q register
7. What mode switch is used to check the acquisition or phase of each distribution pulse?
- a. PROG mode
 - b. INST mode
 - c. A/E mode
 - d. DIST mode
8. The wait light indicates the computer is waiting to:
- a. _____
 - b. _____

- a. Op-code register? _____
- b. D-register? _____
- c. C-register? _____

What registers/circuits control the logic timing of the COM-TRAN Ten?

- a. _____
- b. _____
- c. _____
- d. _____

DUCTION

urpose of this assignment is to provide you with a basic dge of the data flow between the registers of the COM-TR gital computer. A basic understanding of how and in wha ce data are transferred will be required for you to trou the COM-TRAN Ten digital computer successfully.

TOPIC LEARNING OBJECTIVES

EXTRACT troubleshooting and performance data from given and logic diagrams of a general purpose digital comput training device. All circuit performance and operatin characteristics will be documented on job sheets in ac dence with specifications contained in COM-TRAN Ten Te cal Operations Manual M104, Vol. I.

MATCH designated registers of the COM-TRAN Ten with statements that describe the sequence of transfer between them. A copy of the Com-Tran Ten block diagram will be provided as a reference.

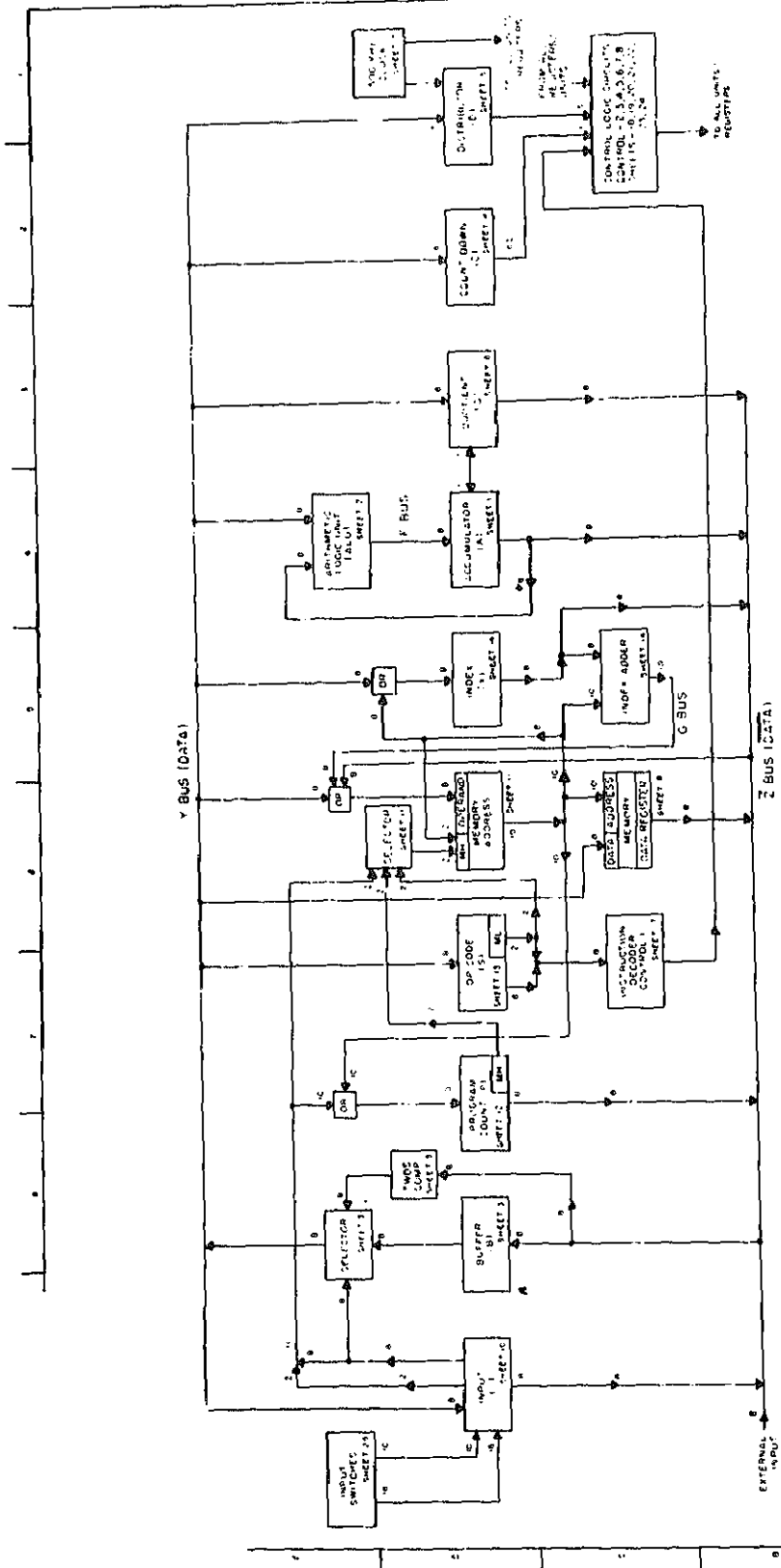
ASSIGNMENT

Notetaking Sheet 5.5.1N and complete all questions.

QUESTIONS

atch the registers of the COM-TRAN Ten digital computer l column A with the statements in column B that describe quence of transfer between them. Refer to the block dia page 28.

A	B
) I-register to B-register	a. Memory to Z-bus to B-register selector to Y-bus to ALU to bus to A-register.
) I-register to memory	b. Memory to Z-bus to B-register selector to Y-bus to S-regis
) I-register to P-register	c. P-register low-order bits to M-register. P-register h order bits to selector to M-register.
) I-register to M-register	d. Memory to Z-bus to B-register selector to Y-bus to Q-regis
) I-register to S-register	



(7) I-register to A-register	f. Memory to Z-bus to B-register selector to Y-bus to X-register
(8) I-register to Q-register	g. Q-register to Z-bus to B-register selector to Y-bus to memory
(9) I-register to C-register	h. A-register to Z-bus to B-register selector to Y-bus to memory
(10) I-register to D-register	i. X-register to Z-bus to B-register selector to Y-bus to memory
(11) P-register to M-register	j. M-register direct transfer to P-register.
(12) Memory to S-register	k. A-register 1 bit transfer to register.
(13) Memory to M-register	l. I-register to selector to S-register.
(14) M-register to P-register	m. I-register to Z-bus to B-register
(15) Memory to teletype	n. I-register low-order bits selector to Y-bus to M-register I-register high-order bits selector to M-register.
(16) Memory to A-register	o. I-register to Z-bus to B-register selector to Y-bus to memory
(17) Memory to Q-register	p. I-register to selector to X-register.
(18) Memory to I-register	q. I-register to selector to ALU to F-bus to A-register
(19) Memory to X-register	r. I-register to selector to Q-register.
(20) X-register to memory	s. I-register to selector to C-register.
(21) X-register to M-register	t. I-register to selector to D-register.
(22) A-register to memory	u. I-register direct transfer bits to P-register.
(23) Q-register to memory	

NOTE: The right column is continued on the next page.

2. What is the purpose of the control 1 instructor (sheet 17)?
-

3. The 2's complementor is used to complement the registers?

a. _____

b. _____

4. What register must all data go through before leaving memory?
-

5. The Z-bus is an input bus for what registers?

a. _____

b. _____

INTRODUCTION

The purpose of this assignment is to familiarize you with the programming steps, flow chart symbols, instruction-word format, instruction repertoire, and machine language of the COM-TRAN Ten.

LEARNING TOPIC LEARNING OBJECTIVES

- .22 MATCH each of the six major steps in programming with the term and definition describing it.
- .23 SELECT, from a given list, the proper order of the steps in programming.
- .24 MATCH the names of flow chart symbols with statements describing them.
- .25 SELECT, from a given list, the statement that describes the difference between a program flow chart and a system flow chart.
- .26 SELECT, from a given list, the statement that describes the difference between mnemonic and machine language.
- .27 SELECT, from a given list, the statement that describes the COM-TRAN Ten instruction-word format.
- .28 MATCH given instructions with statements describing their functions.
- .29 MODIFY the OP CODE, given a list of instructions, to indicate the second, third, or fourth level of memory by writing each code in the appropriate column.
- .30 MODIFY the OP CODE, given a list of instructions, to indicate indexing and the first level of memory by writing each code in the space provided.
- .31 SELECT, from a given list, the purpose of indexing.
- .32 SELECT, from a given list, the statement that describes the operation of a specified Load instruction.
- .33 SELECT, from a given list, the statement that describes the operation of a specified Store instruction.
- .34 SELECT, from a given list, the statement that describes the operation of a specified Arithmetic instruction.

- 11.3.35 SELECT, from a given list, the statement that the operation of a specified Logical instruction.
- 11.3.36 SELECT, from a given list, the statement that the operation of a specified Branch instruction.
- 11.3.37 SELECT, from a given list, the statement that the operation of a specified Input/Output instruction.
- 11.3.38 SELECT, from a given list, the definition of a routine.
- 11.3.39 LIST, with the aid of the HSI and a program of TRAN Ten instructions, the contents of a specified register after each instruction has been executed.

STUDY ASSIGNMENT

Read Notetaking Sheet 5.6.1N and complete the assignment.

STUDY QUESTIONS






- Match each of the programming steps in column A with the definition describing it in column B.

<u>Column A</u>	<u>Column B</u>
___ 1. Step 1	a. <u>Debugging</u> --the process of finding and correcting errors in the program.
___ 2. Step 2	b. <u>Coding</u> --the process of translating the operations in the problem into a language the computer can understand.
___ 3. Step 3	c. Write a clear comprehension of the problem.
___ 4. Step 4	d. <u>Analysis</u> --of the problem to determine which operations are susceptible to arithmetic and logical computation.
___ 5. Step 5	e. <u>Execution</u> --of a program.
___ 6. Step 6	f. <u>Flow chart</u> --A graphic representation in which symbols denoting various operations are arranged showing the sequence of operations to be performed.
	g. <u>Documentation</u> --Is an organized collection of material, flow chart, instructions for the computer and other information about the program.

Put the six steps to programming in their proper order by putting the letter sequencing each term in column B in the appropriate blank in column A.

A	B
___ 1. Step 1	a. Coding
___ 2. Step 2	b. Analysis
___ 3. Step 3	c. Statement
___ 4. Step 4	d. Documentation
___ 5. Step 5	e. Debugging
___ 6. Step 6	f. Flow chart

Match the flow chart symbols in column A with their function in column B.

A	B
___ 6. 	a. Input/output
___ 7. 	b. Connection
___ 8. 	c. Manual input
___ 9. 	d. Decision
___ 10. 	e. Preparation
	f. Termination
	g. Process
	h. Flowline
	i. Pre-defined process
	j. Annotation

- _____ 1. A system flow chart represents a complete the program; whereas, a program flow chart only a portion of the program.
- _____ 2. A system flow chart represents a general of the problem; whereas, a program flow chart presents a step-by-step sequence of the operation of a program.
- _____ 3. A system flow chart represents a general of the problem; whereas, a program flow chart presents a general approach between flow charts and program instructions.

5. Which statement best describes the difference between machine language and mnemonics?

- _____ 1. Machine language is a binary expression that a computer can understand; whereas, mnemonics are alphabetical expressions that label and identify individual instructions.
- _____ 2. Machine language is a numeric expression for an instruction, while a mnemonic is an alphabetical expression for an instruction name given as an aid to memory.
- _____ 3. Machine language is an alphabetical expression for an instruction, while a mnemonic is a numeric expression of an instruction.
- _____ 4. Machine language is an alphabetically expressed instruction; whereas, mnemonics are binary expressions which computers can readily understand.

6. List and define the two parts of the COM-TRAN Ten word.

- 1. _____
- 2. _____

Match the instructions in column A with their function in column B.

<u>A</u>	<u>B</u>
1. LCI	a. Load the A-register with the contents of the memory address indicated by the OPERAND.
2. MNI	b. Branch to the memory address indicated by the OPERAND if condition code ">0" is set.
4. BSB	c. Shift the AQ-register left the number of places indicated by the OPERAND.
5. LAN	d. Increase the contents of the X-register by the value indicated by the OPERAND.
7. BPS	e. Add one to the contents of the memory address indicated by the OPERAND.
8. BST	f. Load the A-register with the 2's complement of the memory address indicated by the OPERAND.
9. MPY	g. Add the contents of the memory address indicated by the OPERAND to the A-register, leaving the result in the A-register.
10. RAO	h. Load the X-register with the value indicated by the OPERAND.
11. DIV	i. Load the C-register with the value indicated by the OPERAND.
12. BUN	j. Multiply the A-register by the contents of the memory address indicated by the OPERAND leaving the results in the AQ-register.
13. LDA	k. Branch unconditionally to the memory address indicated by the OPERAND.
14. SLA	l. Branch to the memory address indicated by the OPERAND and STOP.
15. INX	m. Transfer the contents of the I-register to the memory address indicated by the OPERAND
	n. Divide the AQ-register by the contents of the memory address indicated by the OPERAND, leaving the quotient in the Q-register and the remainder in the A-register.
	o. Store a BUN OP CODE at the memory address indicated by the OPERAND. Store the contents of the P-register at the next memory address after the one indicated by the OPERAND (M+1) then branch to the second memory address after the one indicated by the OPERAND (M+2).

indicate the 2nd, 3rd, or 4th levels of memory by writing the appropriate code in the appropriate column.

	<u>Second level</u>	<u>Third level</u>	<u>Fourth level</u>
1. LAN	_____	_____	_____
2. ADD	_____	_____	_____
3. BST	_____	_____	_____
4. DIV	_____	_____	_____
5. LDA	_____	_____	_____
6. BSB	_____	_____	_____
7. STA	_____	_____	_____
8. MPY	_____	_____	_____
9. RAO	_____	_____	_____
10. BUN	_____	_____	_____
11. BPS	_____	_____	_____

9. Modify the OP CODES of the following instructions to indexing and the 1st level of memory by writing each in the space provided.

1. LAN	_____
2. ADD	_____
3. BST	_____
4. DIV	_____
5. LDA	_____
6. BSB	_____
7. STA	_____
8. MPY	_____
9. RAO	_____
10. BUN	_____
11. BPS	_____

Which statement best describes the purpose of "indexing"?

- ___ 1. A programmer uses indexing to locate a bit of information during the program operation.
- ___ 2. Indexing allows the programmer to repeat an operation throughout a section of memory.
- ___ 3. Indexing is changing a portion of the control memory to allow the selection of specific information.
- ___ 4. Indexing is the selection of the location where certain subroutines will be located.

Which statement best describes the action of the "store" instructions?

- ___ 1. The "store" instructions are all register-to-register operations.
- ___ 2. The OPERAND of the "store" instructions specifies the register that will be acted upon during the execution of the instruction.
- ___ 3. "Store" instructions store the contents of the register specified by the OP CODE into the memory address contained in the OPERAND of the instruction. The contents of the registers are not altered.
- ___ 4. The "store" instructions are immediate addressing instructions; that is, the value in the OPERAND is placed into the specified register upon the execution of the instruction.

Which statement best describes the action of the ADD and SUB instructions?

- ___ 1. The ADD instruction adds the contents of the memory address to the contents of the accumulator and places the result into the memory address specified by the OPERAND.
- ___ 2. The ADD instruction adds the contents of the Q-register to the contents of the accumulator and places the result into the accumulator.
- ___ 3. The ADD instruction adds the contents of the OPERAND to the contents of the accumulator and places the result into the accumulator.
- ___ 4. The SUB instruction subtracts the OPERAND from the OP CODE and places the result into the accumulator.
- ___ 5. The SUB instruction subtracts the contents of the OPERAND from the contents of the accumulator and places the result into the accumulator.

Cont'd on next page)

memory, and the result is placed into the accumulator.

Which statement best describes the action of the MPY instruction?

- _____ 1. The MPY instruction arithmetically multiplies the OPERAND and the memory address specified by the OP CODE and places the result into the accumulator.
- _____ 2. The MPY instruction multiplies the accumulator by the OPERAND and places the product into the AQ register.
- _____ 3. The MPY instruction multiplies the accumulator by the contents of the specified memory address (+1), then logically "ANDS" the result with the previous data in the accumulator.
- _____ 4. The MPY instruction multiplies the contents of the accumulator register with the contents of the memory address and places the results in the AQ-register.

Which statement best describes the action of the DIV instruction?

- _____ 1. The divisor is in the AQ-register and the dividend is in the memory address.
- _____ 2. The OP CODE for the DIV instruction is "78."
- _____ 3. The DIV instruction divides the contents of the AQ-register by the contents of the memory address specified in the OPERAND. The quotient is placed into the Q-register, and the remainder is placed into the accumulator.
- _____ 4. The DIV instruction cannot handle two numbers whose quotient will exceed the bit-length of the Q-register.

Which statement best describes the action of the SLA instruction?

- _____ 1. The SLA works on the AQ-register only.
- _____ 2. The SLA instruction shifts the double-length AQ-register to the right the number of bit positions determined by the OPERAND portion of the instruction. It "pads" the Q-register with zeros.
- _____ 3. The SLA instruction shifts the accumulator to the right and the Q-register to the left in a combined operation that results in all bits being lost, regardless of the count in the OPERAND.
- _____ 4. The SLA instruction shifts the double-length AQ-register to the left for a shift count determined by the OPERAND. It "pads" the low-order bit of the Q-register with zeros.

tion as shown in the program below?

1. The BUN at '70' was generated and stored as a part of the execution of the BSB instruction at location '46'.
2. The OPERAND portion of the instruction word at '70' is the address in the main program to which the computer will branch upon execution of the BSB instruction.
3. The subroutine ends with address '82'.
4. The BUN, '70' at location '82', causes the subroutine to be performed again and again up to a maximum of FF(16) times for each iteration.
5. The OPERAND portion of the instruction word at '82' is the address in the main program to which the computer will return after the completion of the subroutine.
6. The BUN, '70' at memory address '82', sends the program control back to the main program after completion of the subroutine via the BUN, '48' at location '70'.

<u>Program Address</u>	<u>Mnemonic Coding</u>	<u>Comment</u>
'42'	LAI, 00	Make believe initialization of register
'44'	LXI, 0E	other memory locations, in other words
'46'	BSB, 70	a part of previous programming, etc.
'48'	??	BRANCH TO SUBROUTINE. The BSB is generated to send the program to '70'.
..	...	The program continues from this point
..	...	after the completion of the instruction
..	...	in the subroutine.
..	...	
'70'	BUN, 48	The BUN is generated by the BSB, the instruction at '48' is the next instruction after the BSB.
'72'		Beginning of the subroutine instructions.
..		
..		
..		
..		
'82'	BUN, 70	

instruction?

- _____ 1. It informs the computer to output one data block to the peripheral.
- _____ 2. It informs the computer to output a block of data to the peripheral.
- _____ 3. It informs the peripheral to output a block of data to the computer.
- _____ 4. It informs the computer to input a block of data from the peripheral.

8. Which of the following instructions are "input" instructions for the COM-TRAN Ten?

- _____ 1. Write until interrupt (WDI).
- _____ 2. Read data block (RDB).
- _____ 3. Input data block (IDB).
- _____ 4. Read until interrupt (RDI).
- _____ 5. Write data block (WDB).

9. Which statement describes the definition of a "subroutine"?

- _____ 1. A program designed to utilize wasted memory locations in order to fill all memory locations.
- _____ 2. A maxi-program that allows the computer to handle repetitive task.
- _____ 3. A mini-program that allows the computer to handle repetitive tasks.
- _____ 4. A program which allows the computer to handle repetitive tasks.

Analyze the following programs and list the contents of the Accumulator and Quotient after the execution of each instruction.

PROGRAM ADDRESS	OPERATION CODE		OPERAND		ACCUMULATOR
	MNEMONIC	"HEX" CODE	MEMORY ADDRESS M	DATA WORD K	
	LDA	20	08		_____
	SRL	18		03	_____
	ADD	60	09		_____
	BST	98	00		_____
	VARIABLE		1A		
	VARIABLE		05		
					ACCUMULATOR
	LDA	20	4E		_____
	ADD	60	4F		_____
	STA	48	4E		_____
	SLL	13		01	_____
	SUB	68	4F		_____
	STA	48	4F		_____
	BST	98	00		_____
	VARIABLE		07		
	VARIABLE		02		

21. Analyze the following program and list the contents Accumulator and Quotient after the execution of each instruction.

PROGRAM ADDRESS	OPERATION CODE		OPERAND	
	MNEMONIC	"HEX" CODE	MEMORY ADDRESS M	DATA WORD K
200	LCI	01		02
202	MNI	F2	24	
204	LDA	22	24	
206	ADD	62	26	
208	STA	4A	2A	
20A	LDA	22	25	
20C	MPY	72	26	
20E	STQ	5A	2C	
210	LDA	22	25	
212	ADD	62	26	
214	MPY	72	24	
216	SLA	0B		0B
218	SUB	6A	2C	
21A	SRA	10		0B
21C	DIV	7A	2A	
21E	BST	9A	00	
224	VARIABLE		A ← 0A	
225	VARIABLE		B ← 0B	
226	VARIABLE		C ← 04	
22A			A ← C	
22C			BC	

ACC

002	MNI	F0	14	
004	LDA	20	14	
006	BSB	A0	18	
008	STQ	58	16	
00A	LDA	20	15	
00C	BSB	A0	18	
00E	SLA	0B		08
010	ADD	60	16	
012	BST	98	00	
014	VARIABLE	A = 03	B = 04	
016	PRODUCT		M ₃	
018	BUN	(00)	(00)	
01A	STA	48	17	
01C	MPY	70	17	
01E	SLA	0B		08
020	MPY	70	17	
022	BUN	90	18	

INTRODUCTION

The purpose of this assignment is to provide you with a basic knowledge of the operation and logic organization of the COM-TRAN Ten registers and units.

LESSON TOPIC LEARNING OBJECTIVES

- 1.1.18 SELECT, from given lists, COM-TRAN Ten operations specified inputs, and commands and subcommands to various registers and units, using the COM-TRAN Ten logic diagrams.
- 1.1.19 SELECT, from given lists, factors in the logic organization of the COM-TRAN Ten, using the COM-TRAN Ten logic diagrams.

STUDY ASSIGNMENT

Read paragraphs 2-11-1 through 2-11-13 in the HSI. Read Making Sheet 5.7.1N and complete the assignment below.

STUDY QUESTIONS

Refer to logic sheet 7 to answer the following questions:

- 1. What is the count in the two D-type flip-flops (8GA and 8GB) when CP2 is low?

___ A. 00 (gc)

___ B. 01 (gc)

___ C. 10 (gc)

___ D. 11 (gc)

- 2. What is the pulse width of the ENABLE signal?

___ A. 6 microseconds

___ B. 8 microseconds

___ C. 2 nanoseconds

___ D. 16 nanoseconds

Stop the clock, a LOW must be felt on pin 5 of U1
When will this occur?

- ☐ A. When the ENABLE is LOW.
 - ☐ B. When the two D-edge-triggered flip-flops are 1 state.
 - ☐ C. When the two D-edge-triggered flip-flops are 0 state.
 - ☐ D. When SPCK is HIGH.
4. What inputs to the single-shot 6H are required to tri Gray code counter continually?
- ☐ A. A LOW on pin 5 and an upclock on pins 3 and 4
 - ☐ B. A LOW on pin 5 and a downclock on pins 3 and 4
 - ☐ C. A HIGH on pin 5 and an upclock on pins 3 and 4
 - ☐ D. A HIGH on pin 5 and a downclock on pins 3 and 4

Refer to logic sheet 5 to answer the following questions:

5. The true conditions, D0, D1, D2, and D3 are taken from flip-flop output?
- ☐ A. \overline{Q}
 - ☐ B. D
 - ☐ C. Q
 - ☐ D. S

What clocks the D-register through its sequential count

- ☐ A. CP1 upclock
- ☐ B. CP2 upclock
- ☐ C. CP3 upclock
- ☐ D. ENABLE

___ D. Y6

8. What clock pulse clears the I-register loaded from the Y-bus?

___ A. CP1

___ B. CP2

___ C. CP3

___ D. Enable

9. Which hex input switch does not input generates ICLK when pressed?

___ A. Hex F

___ B. Hex 1

___ C. Hex 0

___ D. Hex 9

Refer to logic sheet 3 to answer the following

0. When will the B-register be loaded from the Y-bus?

___ A. When the leading edge of CP2 arrives

___ B. When the trailing edge of CP2 arrives

___ C. When the leading edge of CP2 arrives

___ D. When the trailing edge of CP2 arrives

3, 8C), what is felt at pin 7)?

- ☐ A. Pin 4 input.
- ☐ B. Pin 5 input.
- ☐ C. Pin 6 input.
- ☐ D. One's complement input.

12. If the A and B inputs to the selector are LOW (the condition), what is on the Y-bus?

- ☐ A. The I-register.
- ☐ B. The B-register.
- ☐ C. The complement of the B-register.
- ☐ D. The complement of the I-register.

Refer to logic sheet 8 for the following questions:

13. Which of the following signals are not used to write information into memory?

- ☐ A. \overline{IBS}
- ☐ B. Y-BUS input
- ☐ C. $\overline{M0}$ through $\overline{M9}$
- ☐ D. \overline{ISB}

14. If the data word being read from memory is FF(16), voltage level will be felt at NAND gate 7K-A, pin

- ☐ A. 0 volts
- ☐ B. +5 volts

15. How long is the \overline{IBS} signal on pin 4 of 9L-B?

- ☐ A. 2 microseconds
- ☐ B. 6 microseconds
- ☐ C. 8 microseconds
- ☐ D. As long as the LDA instruction is in the S

What signals are necessary to increment the Memory Address register by 1?

- ☐ A. \overline{TGM} and $\overline{CP3}$
- ☐ B. \overline{TPM} and $CP3$
- ☐ C. \overline{TIM} and $CP2$
- ☐ D. \overline{TBM} and $CP2$

What logic levels are needed on pins 2 and 14 of data selector 13 J to transfer S0 and S1 to M8 and M9?

- ☐ A. Pin 2 HIGH and pin 14 HIGH.
- ☐ B. Pin 2 HIGH and pin 14 LOW.
- ☐ C. Pin 2 LOW and pin 14 HIGH.
- ☐ D. Pin 2 LOW and pin 14 LOW.

From what register/s does the M-register receive information at $\overline{DPA8}$?

- ☐ A. S-register only.
- ☐ B. I-register via the Y-bus.
- ☐ C. B-register and S-register.
- ☐ D. P-register via the Z-bus.

What signals will load the M-register from the Z-bus?

- ☐ A. $\overline{DPA8}$ and $CP2$
- ☐ B. \overline{TMB} and $CP2$
- ☐ C. \overline{TIM} and $\overline{CP3}$
- ☐ D. \overline{TPM} and $CP2$

20. What signals are necessary to add the Index register to the M-register and transfer the results to the M-register?
- ☐ A. TXB
 - ☐ B. $\overline{\text{TMX}}$ and CP2
 - ☐ C. LX and CP2
 - ☐ D. AXM, $\overline{\text{TGM}}$, and $\overline{\text{CP3}}$
21. What happens if the sum of the Index register and the M-register exceeds 10-bit places?
- ☐ A. The Index register end carries.
 - ☐ B. The overflow bits are lost.
 - ☐ C. The carry light is set.
 - ☐ D. The ADD overflow light is set.
22. What logic levels are felt on pins 1, 3, 8, and 11E and 11D when the AXM signal is LOW?
- ☐ A. The contents of the X-register.
 - ☐ B. 11111110 (2)
 - ☐ C. 00000001 (2)
 - ☐ D. 00000000 (2)

Refer to logic sheet 12 to answer the following questions.

23. What signals are needed to load the P-register from the M-register?
- ☐ A. $\overline{\text{TMP}}$ LOW, $\overline{\text{TIP}}$ HIGH, and CP2.
 - ☐ B. $\overline{\text{TMP}}$ HIGH, $\overline{\text{TIP}}$ HIGH, and CP2
 - ☐ C. $\overline{\text{TIP}}$ LOW, TPLB, and CP2.
 - ☐ D. $\overline{\text{TMP}}$ LOW, $\overline{\text{TIP}}$ LOW, and CP2.

ಎಂಬುವಂತಾಯಿತು ಇವಳಿಗೆ. ಕೃಷ್ಣಪ್ರೇಮದ ಪರಾಕಾಷ್ಠೆಯಲ್ಲಿರುವವಳು ಇವಳು. 'ಕಾಚಿದಾವಸಥಸ್ಯಾಂತೇ ಸ್ಥಿತ್ವಾ ದೃಷ್ಟ್ವಾ ಬಹಿರ್ಗೌರವಂ | ತನ್ನಯತ್ವೇನ ಗೋವಿಂದಂ ದಧೌ ಮೀಲಿತಲೋಚನಾ ||' ಎಂದೂ 'ಯಯೌ ಚ ಕಾಚಿತ್ ಪ್ರೇಮಾಂಧಾ ತತ್ಪಾರ್ಶ್ವಂ ಅವಿಳಂಬಿತಂ' ಎಂದೂ ಹೇಳಿರುವಂತಾಯಿತು ಇವಳ ದೇಶ. 'ಪ್ರೇಮದಿಂದ ಕತ್ತಲೆ ಕವಿದಿತು. ಆ ಕತ್ತಲೆಯೇ ದಾರಿ ತೋರಿಸಲು ಅವಳು ಅವನ ಬಳಿ ಸಾರಿದಳು'—ಎಂದೂ ಕಂಡು ಬರುತ್ತದೆ. ಅವಳನ್ನು ಎಲ್ಲರೂ ನಿಂದಿಸುತ್ತಿರಬೇಕಾದರೆ ಅವಳು ಹೇಳುವುದೇನು ಎಂದರೆ 'ಅಶ್ವರ್ಯ ಗುಣಬೀಜ್ಞತನೇ, ಮಾಧವನೇ'—ಎಂದೂ. 'ನಿನ್ನನ್ನು ಪರಮ ಪ್ರಣಯಿಯನ್ನಾಗಿ ಮಾಡುವ ಶ್ರೀದೇವಿಗೆ ವಲ್ಲಭನೇ'—ಎಂದೂ ಹೇಳಿಕೊಳ್ಳುತ್ತಾಳೆ.

ಆಶ್ರಿತರಿಗಾಗಿ ನೂರಾರು ಬಗೆಯಲ್ಲಿ ಜನಿಸಿದರೂ 'ನಾನೇನೂ ಮಾಡಲಾಗಲಿಲ್ಲವಲ್ಲ! 'ಮುಣಂ ಪ್ರವೃದ್ಧಂ ಇವ'—ಎಂದು ಹೇಳುವ ಸ್ವಭಾವದವನಾಗಿ ಆಶ್ರಿತರ ಬಗೆಗೆ ವ್ಯಾಮೋಹವನ್ನುಳ್ಳವನು ಅವನು. ತನ್ನನ್ನು ಸ್ಮರಿಸಿದವರ ಜನ್ಮವನ್ನು ಕಳೆದು ಹಾಕುವ ಪ್ರಭಾವವುಳ್ಳ ಶ್ರೀನಾಮಗಳನ್ನು ಉಳ್ಳವನು. ದುಃಖನಿವರ್ತಕವಾದ ಆ ನಾಮಗಳು ಇವಳಿಗೆ ದುಃಖವನ್ನುಂಟು ಮಾಡುತ್ತಿವೆ! 'ರಕ್ಷಿತಾ ಜೀವಲೋಕಸ್ಯ' ಎಂಬುವ ಓರಿವೆ ಇವನದೂ ತನ್ನ ಅನ್ಯಶಂಸ್ಯವನ್ನು ಕೊಂಡಾಡದ ನಿತ್ಯಸೂರಿಗಳಿಗೆ ನಿತ್ಯವೂ ಸೇವೆಯನ್ನು ಕೊಡುವವನು ಇವನು. ಇವಳ ಬಗೆಗೆ ಅವನು ಮಾಡಿದ ಅನ್ಯಶಂಸ್ಯ ವ್ಯಾಪಾರಗಳನ್ನು ನನ್ನಿಂದ ಹೇಳಿ ಮುಗಿಸುವುದಕ್ಕಾಗುವುದಿಲ್ಲ!—

ಶಂದೋಡು ಕಟಲ್ ಮರುನಾಳ ಹೈಂಗೆಳಿಯೆಂನಾ

ಪಾಲೂಟ್ಟುಳ್ ಪಾನ್ಯೆಪೇಣಾಳ

ನಂದಾನೋ ತಿರುವರೆಂಗಂ ಮಾರಾನೋ

ನಿನ್ನೆನೇ ವಳ್ಳಿಯೆಂ ಶೋರುಂ

ಶಂದೋಹನ್ ಪಾಚಿಯೆನ್ ಏನ್ನ ಅಲಲ್ ಓಂಬು

ತೈತ್ತಿರೀಯನ್ ಶಾಮನೇದಿ

ಅನ್ನೋ ವನ್ನು ಎನ್ಮಹಳ್ಳಿ ಶೆಯ್ ದನಹಳ್ಳ

ಅಮ್ಮನೈಮೀರ್ ಅರಿಹಲೇನೇ ||೯||

(ಪಂದೋಡು ಕಟಲ್ ಮರಂವಾಳ್) ನನ್ನ ಮಗಳು ಚಂಡನ್ನೂ ಕಾಲಂದುಗೆ ಯನ್ನೂ ಮುಟ್ಟುವುದಿಲ್ಲ. (ಪೈಕಿಳಿಯಂಬಾಲೂಟ್ಟಾಳ್) ತನ್ನ ಚೆಲುವಾದ ಗಿಳಿಗೆ ಹಾಲನ್ನು ಕುಡಿಸುವುದೂ ಇಲ್ಲ. (ಪಾವೈಪೇಣಾಳ್) ಅಟಕ್ಕಿ ತಕ್ಕು ದಾದ ಮರದ ಬೊಂಬೆಯ ಕಡೆ ನೋಡುವುದೂ ಇಲ್ಲ. (ತಿರುವರಂಗಂ ವಂದಾನೋ ವಾರಾನೋ ಎನ್ನು ಎನ್ನೇ) ಶ್ರೀರಂಗನಾಥನು ಬಂದುಬಿಟ್ಟನೇ ? ಬರಲಾರನೋ ? ಎಂದು ಹೇಳಿಕೊಂಡು (ವಳ್ಳಿಯುಂ ಶೋರುಂ) ಕೈಬಳೆಗಳು ಜಾರಿ ಬೀಳುತ್ತಿರಲು ನಿಂತೇ ಇದ್ದಾಳೆ. (ಶಂದೋಹನ್) ಛಾಂದೋಗ್ಯೋಪ ನಿಷತ್ಪತಿಪಾದ್ಯನೂ (ಪೌಬಿಯನ್) ಕೌಷೀತಕಿ ಬ್ರಾಹ್ಮಣ ಪ್ರತಿಪಾದ್ಯನೂ, (ಐನ್ನು ಅಟಲ್ ಓಮ್ಮು) ಪಂಚಾಗ್ನಿಗಳಿಂದ ಆರಾಧಿಸಲ್ಪಡುವವನೂ, (ತೈತ್ತಿ ರೀಯನ್) ತೈತ್ತಿರೀಯೋಪನಿಷತ್ಪತಿಪಾದ್ಯನೂ (ಶಾಮವೇದಿ) ಸಾಮವೇದ ಪ್ರತಿಪಾದ್ಯನೂ ಆದ ಪಠವಾತ್ಮನು (ಮದು) ಈ ಜಾಗಕ್ಕೆ ಬಂದು (ಎನ್ ಮಹಳ್ಳಿ ಶೆಯದನಹಳ್ ಆಮ್ಮನೈವೀರ್, ಅರಿಹಿಲೇನ್, ಅನ್ನೋ) ನನ್ನ ಮಗಳ ವಿಷಯದಲ್ಲಿ ವಣ್ಣಿಸಿದುದನ್ನು, ತಾಯಿಯರೇ, ನಾನು ತಿಳಿಯಲಾರದವ ಳಾಗಿದ್ದೇನೆ !

ನಿದ್ರಿಸುವ ಸಮಯದಲ್ಲಿಯೂ ನನ್ನ ಮಗಳು ಚಂಡನ್ನೂ ಗೆಜ್ಜೆಯನ್ನೂ ಕೈ ಬಿಡದೆ ಇದ್ದವಳು ಈಗ ಅವುಗಳನ್ನು ಮುಟ್ಟುವುದೂ ಇಲ್ಲ. ತನ್ನ ಮುದ್ದಿನ ಗಿಳಿಗೂ ಹಾಲೂಡಿಸುವುದಿಲ್ಲ. ಅಟದ ಬೊಂಬೆಯನ್ನು ಕಣ್ಣೆತ್ತಿಯೂ ನೋಡುವುದಿಲ್ಲ. 'ಬಾಲ್ಯೇ ಕ್ರೀಡನಕಾಸಕ್ತಾಃ ಯೌವ್ವನೇ ವಿಷಯೋನ್ಮುಖಾಃ | ಅಜ್ಞಾ ನಯಂತ್ಯಶಕ್ತ್ಯಾಚಿ ಮಾರ್ಧಕ್ಯಂ ಸಮಂಪಸ್ಥಿತಾಃ || ತಾಸ್ಮಾದ್ಬಾಲ್ಯೇ ವಿವೇಕಾತ್ಮಾ ಯತೇತ ಶ್ರೇಯಸೇ ಸದಾ !' ಎಂಬುವುದಕ್ಕನುಗುಣವಾಗಿ ಎಲ್ಲ ವನ್ನೂ ಬಿಟ್ಟಂತೆ ಕಾಣುತ್ತದೆ. ಹೀಗೆ ಬಿಟ್ಟವರು ಯಾರಾದರೂ ಉಂಟೋ ಎಂದರೆ 'ಪರಿತ್ಯಕ್ತಾಮಯಕಾಲಂಕಾ' ಎಂದು ವಿಭೀಷಣನ ಬಗೆಗೆ ಕಾಣಬಹುದು; ಅವನೇ ಪ್ರಾಪ್ಯವೆಂಬ ಅರಿವು ಮೂಡಲು ಉಳಿದವೆಲ್ಲಾ ಪ್ರಾಪ್ಯಾಭಾಸಗಳಾಗಿ ತ್ಯಾಜ್ಯವಾಗುವವಷ್ಟೇ ? ಅವನು ಬರುವುದು ನಿಶ್ಚಿತವೆಂದೇ ಇದ್ದಾಳೆ. ಅವನು ಬಂದು ಮುಖ ತೋರನೇ ? ನಾನು ಈ ದಶೆಯೊಡನೆ ಮುಗಿದು ಹೋಗುವುದಷ್ಟೇಯೇ ? ಅಟದ ಬೊಂಬೆಗಳೋಪಾದಿ ಕೈಬಳೆಯೂ ಕಳಚಿ

ಬಿದ್ದಿತು. 'ಅನುರಾಗೇಣ ಶೈಥಿಲ್ಯಮಸ್ಥಾಸು ವ್ರಜತೋ ಹರೇಃ | ಶೈಥಿಲ್ಯ ಮಂಪಯಶಾಂತಾಶು ಕರೇಷು ವಲಯಶಾನ್ಯಪಿ ||' ಎಂಬಂವಂತಾಯಿತು.

ಈ ಕೆಲಸವನ್ನು ಒಬ್ಬ ಅಜ್ಞಾನು ಮಾಡಿದ್ದರೆ ಸಹಿಸಿಕೊಳ್ಳಬಹುದಾಗಿತ್ತು. 'ವೇದೈಶ್ಚ ಸರ್ವೈರಹಮೇವ ವೇದ್ಯಃ ವೇದಾಂತವಿದ್ವೇದವಿದೇವ ಚಾಹಂ'—ಎನ್ನುವ ಹಿರಿಮೆಯನ್ನುಳ್ಳ ಸರ್ವಜ್ಞನೇ ಈ ರೀತಿ ಮಾಡಿದವನು ! ಒಬ್ಬನು ಅವಿವೇಕಿ ಮಾಡುವಂತೆ ಸರ್ವಜ್ಞನು ಮಾಡಿದರೆ ನಾನೆಲ್ಲಿ ತಾನೇ ಹೋಗಿ ಸೇರಬಲ್ಲೆ ? ಅವನೇ ಬಂದು ಹೀಗೆ ಮಾಡಿಬಿಟ್ಟು ತಾನೇ ಉಪೇಕ್ಷಿಸಬಹುದೇ ?

ಶೇಲ್ ಉಹಳಂ ವಯಲ್ ಪುಡೈತೂಟ್

ತಿರುವರಂಗತ್ತಮ್ಮಾನ್ನೈ ಶಿಂದೈಶೆಯಾದ

ನೀಲಮಲರ್ ಕಣ್ ಮಡವಾರ್ ನಿರೈಅಟುವೈ

ತಾಯ್ ಮೊಟಂದ ಅದನ್ನೈ ನೇರಾರ್

ಕಾಲನೇಲ್ ಪರಕಾಲನ್ ಕಲಿಕನ್ನಿ

ಒಲಿಮಾಲ್ಯೈ ಕತ್ತುವಲ್ಲಾರ್

ಮಾಲ್ಯೈಶೇರ್ ವೆಣ್ ಕುಡೈಕೀಟ್ ಮನ್ನರಾಯ್

ಪೊನ್ನೂಲಹಿಲ್ ವಾಟ್ ವರ್ ತಾನೋ ||೧೦||

(ಶೇಲ್ ಉಹಳಂ) ಮೀನುಗಳು ಚಿಮ್ಮಿನಲಿಯುತ್ತಿರುವಂಥ (ವಯಲ್ ಪುಡೈ ಶೂಟ್) ಗದ್ದೆಗಳಿಂದ ಸುತ್ತಲೂ ಸುತ್ತುವರಿಯಲ್ಪಟ್ಟಿರುವ (ತಿರು ಅರಂಗತ್ತು ಅಮ್ಮಾನ್ನೈ) ಶ್ರೀರಂಗದಲ್ಲಿರುವ ಸ್ವಾಮಿಯನ್ನು (ಶಿಂದೈಶೆಯಾದ) ಧ್ಯಾನಿಸಿಕೊಂಡಿರುವ (ನೀಲಮಲರ್ ಕಣ್ ಮಡವಾರ್) ಕನ್ನೈದಿಲೆಯಂತೆ ಕಣ್ಣುಗಳನ್ನುಳ್ಳ ಪರಕಾಲನಾಯಕಿಯ (ನಿರೈಅಟುವೈ) ಲಜ್ಜೆ, ನಾಣು ಇವುಗಳೂ ಅಳಿದುಂದನ್ನು ಕುರಿತು (ತಾಯ್ ಮೊಟಂದ ಅದನ್ನೈ) ತಾಯಿ ಹೇಳಿದ ಮಾತುಗಳ ರೂಪದಲ್ಲಿ (ನೇರಾರ್ ಕಾಲನ್) ಶತ್ರುಗಳಿಗೆ ಯವನಂತಹವರೂ, (ವೇಲ್) ವೇಲಾಯುಧ ಧಾರಿಗಳೂ (ಪರಕಾಲನ್) ಪರಕಾಲರನ್ನವ ಶ್ರೀನಾಮವನ್ನುಳ್ಳವರೂ, ಆದ (ಕಲಿಕನ್ನಿ) ತಿರುಮಂಗೈ ಅಳ್ವಾರ್ ಅವರು (ಒಲಿ ಮಾಲ್ಯೈ) ಹಾಡಿದ ಈ ನುಡಿಮಾಲೆಯನ್ನು (ಕತ್ತುವಲ್ಲವರ್ ತಾಮ್) ಓದಿ ಅರಿಯ ಬಲ್ಲವರು (ಮಾಲ್ಯೈಶೇರ್ ವೆಣ್ ಕುಡೈಕೀಟ್) ನುಡಿಸಿನ ಸರಗಳು

ತೂಗಾಡುವ ಶ್ವೇತಚ್ಚತ್ರದ ನೆರಳಿನಲ್ಲಿ (ಪಂನ್ನವರ್ ಅಯ್) ರಾಜರಂಗಳಾಗಿದ್ದು ಕೊಂಡು ಈ ಲೋಕದ ಐಶ್ವರ್ಯವನ್ನು ಅನುಭವಿಸಿದ ನಂತರ (ಪೊನ್ ಉಲ ಹಿಲ್ ವಾಟರ್ ವರ್) ಪರಮಪದದಲ್ಲಿ ನಿತ್ಯಾನುಭವವನ್ನು ಮಾಡುವವರಾಗುತ್ತಾರೆ.

ತೀರ್ಥಕ್ಕುಗಳೂ ಸಹ ನಲಿದಾಡುವಂತಹ ಗದ್ದೆಗಳಿಂದ ಸುತ್ತವರಿಯಲಟ್ಟಿ ಶ್ರೀರಂಗದಲ್ಲಿರುವ ಸರ್ವೇಶ್ವರನನ್ನು ಧ್ಯಾನಿಸುತ್ತಾ ತನ್ಮಯಳಾದ ಪರಕಾಲ ನಾಯಕಿ ತನ್ನ ಸ್ತ್ರೀತ್ವವನ್ನು ಅಳಿಸಿಕೊಂಡ ಬಗೆಯನ್ನು ಅವಳ ತಾಯಿಯ ನುಡಿಗಳಲ್ಲಿ ನಿರೂಪಿಸಿದ್ದಾರೆ ಆಳ್ವಾರ್ ಅವರು. ಈ ಆತ್ಮ ಸಂದರ್ಭವನ್ನು ಸಮೀಚೀನರಾದ ಆಚಾರ್ಯರ ಉಪದೇಶದಿಂದ ಅರಿಯುವವರು ಪರಮಾತ್ಮನ ಶ್ವೇತಚ್ಚತ್ರಿಯ ನೆರಳಲ್ಲಿ ಸಾರುವವರಾಗಿ, ಅವನ ಕೈಯಿಂದಲೇ ಮಾಲೆಯನ್ನು ಪಡೆಯಬಲ್ಲ ಸ್ವರೂಪಿಗಳಾಗಿ ಶ್ರೀವೈಕುಂಠದಲ್ಲಿ ಭಗವಂತನ ನಿತ್ಯಾನುಭವವನ್ನು ಮಾಡುವವರಾಗಿ ಬಾಳುತ್ತಾರೆ.

ತಿರುಮಂಗೈ ಆಳ್ವಾರ್ ತಿರುವಡಿಹಳ್ಳೇ ಶರಣಂ